REMARKS

This paper is responsive to the Non-Final Office Action dated March 22, 2005. Claims 1-46 were examined.

The informalities noted by the Examiner with respect to claims 5and 6 and 42 and 43 have been corrected. Accordingly, applicants respectfully request that the objection to those claims be withdrawn.

Claims 1, 2, 6-10, 16, 17, 26-30, 35, and 38 stand rejected under 35 U.S.C § 102(b) as being anticipated by Estakhri (US 6,404,246). Claims 11, 12, 18, 21-23, 31, 36, 37, 39, 42, and 43 stand rejected under 35 U.S.C § 103 as unpatentable over Estakhri. Applicant appreciates that the Office Action indicates that claims 3-5, 13-15, 19, 20, 24, 25, 32-34, 40, 41 and 44-46 contain allowable subject matter.

Claims 3 and 6 were amended to correct informalities and claims 3 and 5 were amended to conform to changes to claim 1. Claim 22 was amended to conform to changes to claim 21. Claim 28 was amended to conform to amendments made to claim 26. Claims 44-46 were amended to conform to the amendments made to claim 42 and/or to correct informalities noted in review. Claims 8 and 9 have been canceled.

With respect to amended claim 1, applicants respectfully submit that Estakhri fails to teach generating at least one control value in a control loop to lock a clock generated by a controllable oscillator to a multiple of the calibration clock. Instead Estakhri teaches using calibration system 2002 shown in Fig. 2, which is not taught to be a control loop. As described at col. 4, line 66 to col. 5, line 15, the frequency comparator compares the frequency of the VCO clock 208 to the precision external clock. The output of the comparator 216 is used to generate a new count value which is loaded in the register 212, which controls the frequency of the VCO clock 208. There is no teaching that the new count value is generated in a control loop (e.g. a phase-locked loop as specifically recited in claim 2) or that the calibration system 2002 is part of a control loop. Accordingly applicants submit that claim 1 and all claims dependent thereon distinguish over Estakhri.

With respect to amended claim 21, applicants respectfully submit that Estakhri fails to teach generating a control value in a control loop of the device to cause the controllable oscillator to lock to a multiple of the calibration clock. Instead Estakhri teaches using calibration system 2002 shown in Fig. 2. As described at col. 4, line 66 to col. 5, line 15, the frequency comparator compares the frequency of the VCO clock 208 to the precision external clock. The output of the comparator is used to generate a new count value which is loaded into the register 212, which controls the frequency of the VCO clock 208. There is no teaching that the new count value is generated in a control loop or that the calibration system 2002 is part of a control loop. Accordingly applicants submit that claim 21 and all claims dependent thereon distinguish over Estakhri.

With respect to amended claim 26 applicants respectfully submit that Estakhri fails to teach a phase-locked loop circuit that includes the controllable oscillator and that the phase-locked loop circuit is coupled to receive the calibration clock signal and generate a correction factor to cause the controllable oscillator to lock to a multiple of the calibration clock signal. Instead Estakhri teaches using calibration system 2002 shown in Fig. 2. Estakhri does not teach that the calibration system 2002 includes the clock synthesizer 2000 in a phase-locked loop. At col. 4, line 66 to col. 5, line 15, Estakhri describes calibration system 2002 in which the frequency comparator 216 compares the frequency of the VCO clock 208 to the precision external clock 218. The output of the comparator is used to generate a new count value which is loaded into the register 212, which controls the frequency of the VCO clock 208. There is no teaching that a new count value is generated in a phase-locked loop circuit that includes the controllable oscillator or that the calibration system 2002 is part of a phase-locked loop circuit that includes the clock synthesizer 2000. Accordingly, applicants submit that claim 26 and all claims dependent thereon distinguish over Estakhri.

With respect to claim 42 applicants submit that Estakhri fails to teach means for calibrating the apparatus utilizing a calibration clock supplied on the terminal by internally generating, in a phase-locked loop, one or more control values for the controllable oscillator. As pointed out above, Estakhri fails to teach generating control values such as the count value for the count value register in a phase-locked loop. Instead, Estakhri teaches using calibration system 2002 shown in Fig. 2. As described at col. 4, line 66 to col. 5, line 15, the frequency

comparator 216 compares the frequency of the VCO clock 208 to the precision external clock. The output of the comparator is used to generate a new count value which is loaded into the register 212, which controls the frequency of the VCO clock 208. However, that fails to teach a new count value being generated in a phase-locked loop. Accordingly applicants submit that claim 42 and all claims dependent thereon distinguish over Estakhri.

New claims 47 and 48 are being added to claim additional features of the invention. Claim 47 is similar to the subject matter recited in claim 3, which was indicated as allowable. Claim 48 depends on claim 47.

In summary, claims 1-7 and 10-48 are in the case. All claims are believed to be allowable over the art of record, and a notice to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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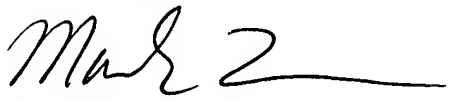

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